Design of Low Pass Filter using Split Ring Resonator shaped Defected Ground Structure

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Abstract:

This paper deals with the design of a Low Pass Filter using Split Ring Resonator (SRR) shaped Defected Ground Structure (DGS). This paper primarily focuses on the analysis and design of Low pass filter using DGS with the aid of a 3D EM software simulation tool. The designed/fabricated filter has 3dB cutoff frequency at 10.9 GHz. The insertion loss in the pass-band is less than 1.5 dB from DC to 10.4 GHz. And the rejection levels are greater than 20 dB from 12 to 20 GHz. This article provides an in-depth analysis of unit element and cascaded stage of DGS used to realize a low pass filter.

Keywords: Split Ring Resonator (SRR), Defected Ground Structure (DGS), Low Pass Filter (LPF)

I INTRODUCTION

In today's high-performance radar systems, compact, low-cost and high-performance microwave filters are highly desirable. To meet the requirements like harmonic suppression, spurious rejection and rejection of transmitted leak signal, we need to develop different kinds of filters. Among them, it is well known that **D**efected **G**round **S**tructure (DGS) based filters typically have characteristics of rejecting the incoming signals in a particular frequency band of interest. DGS is realized by etching off a periodic defected pattern (usually different kinds of dumbbell shaped, split ring resonators) from the metallic ground plane, which is the rear side of the PCB. This DGS unit will change the distribution of current in the ground plane, thereby resulting in the equivalent capacitance and inductance of transmission line [1-2].

Making the defected pattern on the ground plane increases current path, thus increasing the inductance per unit length of the line. Increase in inductance results in the increase of the line impedance [3]. DGS affects not only the inductance but also the capacitance. In the standard micro-strip line, the electric and magnetic fields are confined between the line and the ground plane, at a distance ruled by line width, dielectric constant and the thickness of the substrate. But when the defect is placed in the ground plane beneath the line, the fields get disturbed, resulting in an increased distance and hence a lower capacitance. The low capacitance is another factor which increases the line impedance. Therefore the effect of both inductance and capacitance makes the line impedance to increase.

II DESIGN OF SINGLE ELEMENT OF DGS

The proposed SRR shaped DGS is obtained by etching the ground plane with two concentric split-rings which have different size. The inner split ring is placed within the outer split ring in a reverse direction as shown in ***Figure 1*** [5-6]. The micro-strip line on top side has a characteristic impedance of 50 Ω. In the present design, the substrate used has a dielectric constant (ε_r) of 2.33, loss tangent of 0.0012 and the substrate height (h) of 0.254mm.

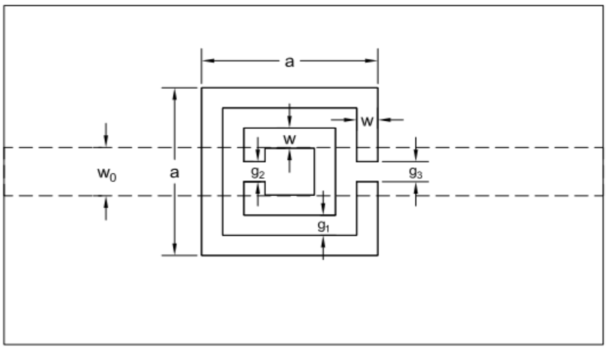
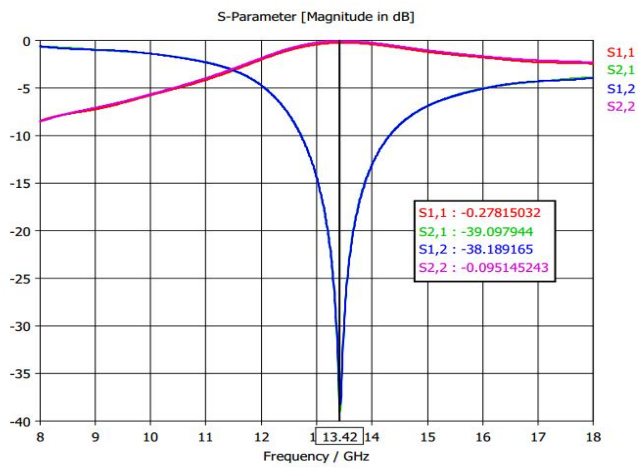


Figure 1 Bottom view of single element DGS with micro-strip line



The proposed SRR-shaped DGS has been simulated using a commercially-available 3D EM software tool CST MW Studio [7]. The simulated s-parameters are shown in ***Figure 2*** which brings out the band rejection property of the proposed single DGS structure.

Figure 3 & ***Figure 4*** show the simulated S-parameters with variation of parameter **a** (refer ***Figure 1***). As the length of **a** increases, the effective series inductance of the line increases, resulting in a lower cutoff frequency.

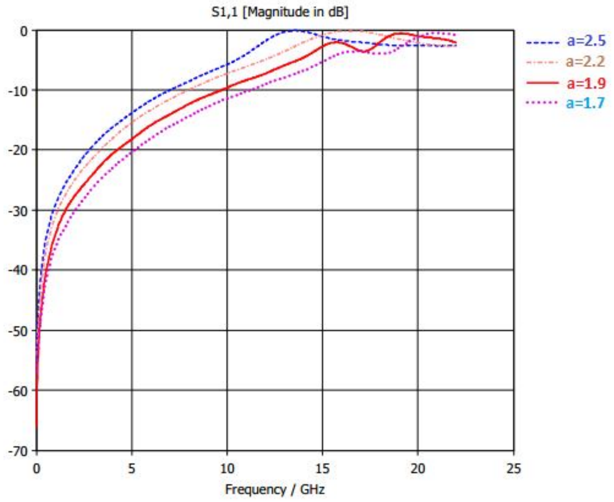


Figure 3 Simulated S-Parameter (S11) with variation of parameter **a**

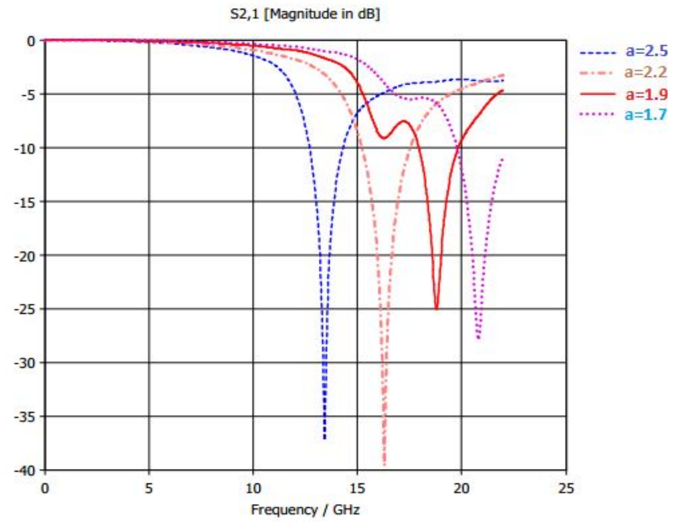


Figure 4 Simulated S-Parameter (S21) with variation of parameter **a**

III EQUIVALENT CIRCUIT OF DGS

Cutoff and attenuation pole characteristics of the DGS section can be determined using the S-parameters obtained from EM simulation of single element of DGS. The circuit parameters extracted from the simulation results can be fitted for a one-pole Butterworth-type low-pass response. The LC equivalent of DGS is shown in ***Figure 5***.

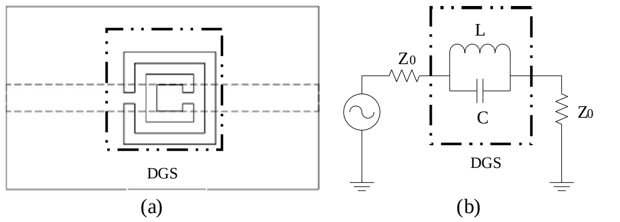


Figure 5 (a) DGS Single element (b) LC Equivalent circuit

The equivalent inductance and capacitance are given as [8]

$$L = \frac{1}{4\pi^2 f_o^2 C} \quad (1)$$

$$C = \frac{f_c}{2Z_o} \cdot \frac{1}{2\pi(f_0^2 - f_c^2)} \quad (2)$$

where f_0 is the resonant frequency of LC resonator and f_c is the 3dB cutoff frequency.

IV DESIGN OF LPF USING PROPOSED DGS

The specifications of the LPF are given below

3dB Cutoff frequency: 10.9 GHz
Pass band: upto 10.6 GHz
Pass band Insertion Loss: 1.5 dB (max)
Rejection: 20 dB (min) @ 12 GHz - 18 GHz

From the previous section, the parameter **a** of the SRR-shaped DGS primarily controls the shift in rejection frequency. Therefore multiple stages of single element were cascaded (as in ***Figure 6***), with fine adjustments of the other parameters, to get the desired result.

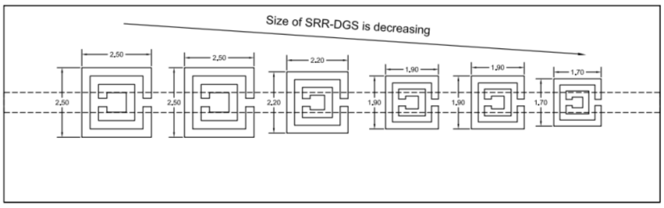


Figure 6 Cascaded elements of DGS

This low pass filter has been simulated on an RF substrate material -- RT/duroid 5870, which has a PTFE/glass/ceramic dielectric. This substrate is characterized by its dielectric constant (εr) of 2.33, loss tangent of 0.0012 and dielectric height (h) of 0.254mm.

The top side of the PCB has only a 50 Ω line, while the bottom side has the periodic structure of split ring resonator-shaped DGS of varying sizes etched in copper.

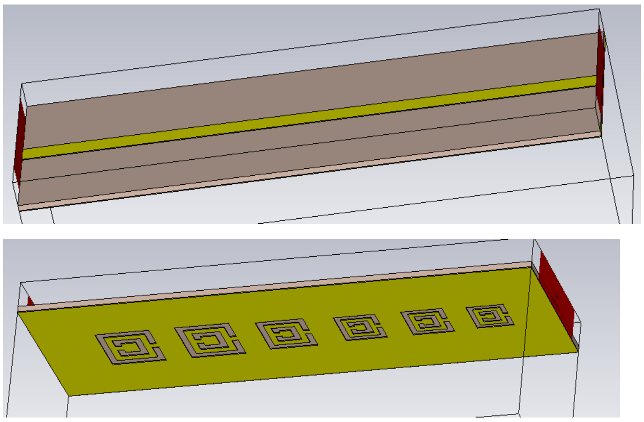
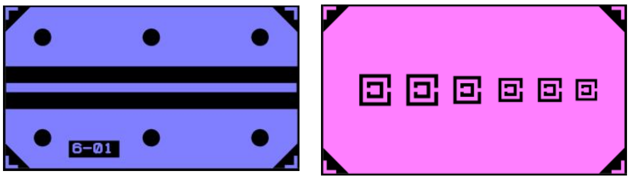


Figure 7 3D view for EM simulation

A 3D view of designed filter is shown in ***Figure 7*** which was simulated using the 3D EM software tool. The PCB layout view of designed filter is shown in ***Figure 8***. As shown in ***Figure 9***, the 3dB cutoff frequency is 10.9GHz, insertion loss is 1dB up to 10.6GHz.



(a) Top Side (b) Bottom Side

Figure 8 Layout view of designed LPF

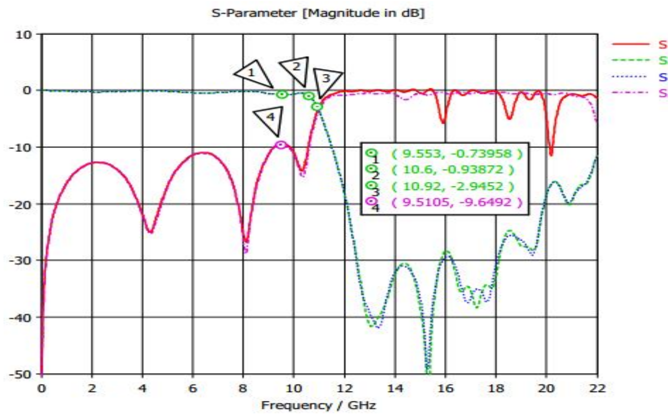


Figure 9 EM Simulation Results for LPF

Figure 10 depicts the photograph of the fabricated DGS-based LPF, including a precision mechanical structure designed to form a test jig for design validation.

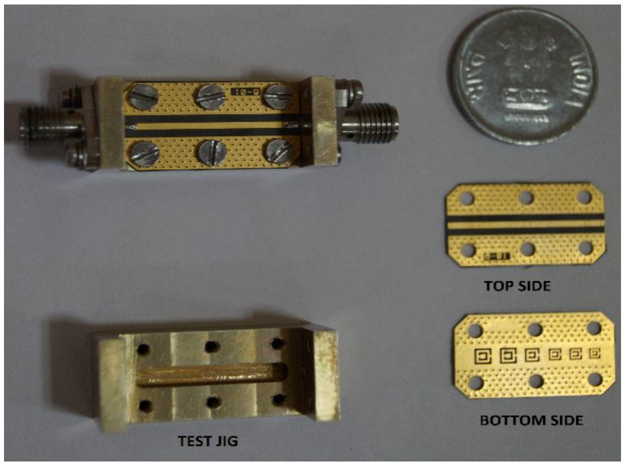


Figure 10 Photograph of DGS-based LPF

Figure 11 Measurement setup

The S-parameters have been measured using a Vector Network Analyzer (VNA) as shown in ***Figure 11***. ***Figure 12*** shows the measured results for the fabricated filter.

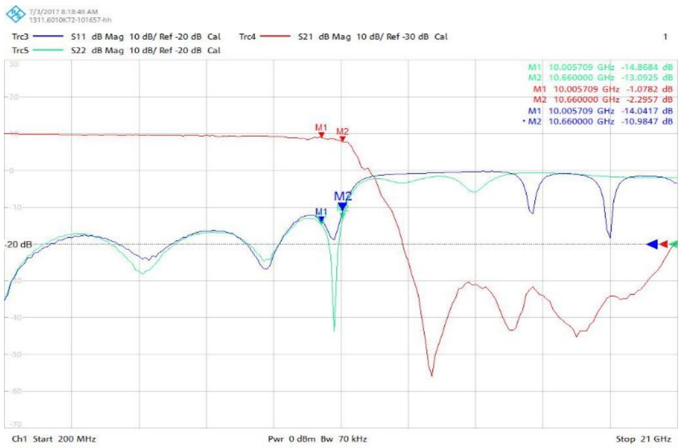


Figure 12 Measured Results

Figure 13 shows a comparison of the measured results with the simulated results. Here, the insertion loss includes the loss of two SMA connectors which are used for measurement in the test jig. *The measured results match well with the simulation results.*

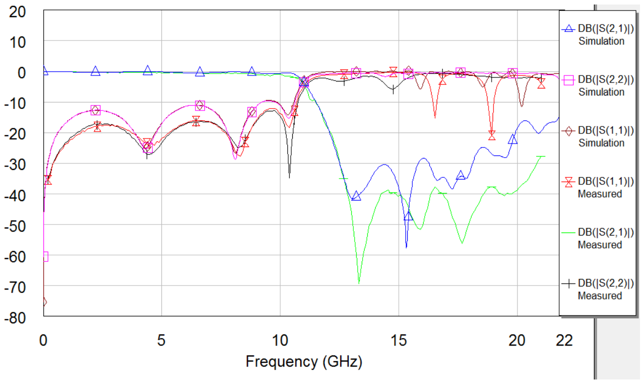


Figure 13 Comparison of Simulated and Measured Results

CONCLUSION

In this low pass filter design, first a single element of DGS was simulated using 3D EM software. Then, using parameter sweep, the characteristics of this single element of DGS were analyzed. It was observed that the frequency of rejection changed with change in parameters of the DGS cell. Then, finally, a cascaded structure of unit DGS was made in the bottom layer of PCB to get the desired rejection in the stop band. It was fabricated & tested on a precision test jig, with very good correlation between practical measurement and simulation results.

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